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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,014	01/29/2002	Chong Lee	174/211	5565

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EXAMINER	
WANG, TED M	
ART UNIT	**PAPER NUMBER**
2611	
MAIL DATE	**DELIVERY MODE**
05/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/059,014	LEE ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 11-16, 24 ands 25* is/are rejected.

7)☒ Claim(s) *2-10, 17-23 and 26-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's amendments and arguments, filed 02/28/2007, with respect to the rejection(s)of claim(s) 1-3, 6-18, and 22-26 under 35 U.S.C. 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kyles et al. (US 6,008,680).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 16, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyles et al. (US 6,008,680).

- With regard claim 1, Kyles et al. discloses Circuitry for using a reference clock signal to extract data from a data signal (Fig.5 element 510 and RECEIVE DATA and RECOVERED CLOCK) comprising:

  first circuitry (Fig.5 element 300) configured to derive from the reference clock signal (Fig.53 element MASTER CLOCK) first and second phase-shifted versions of the reference clock signal (Fig.5 elements CLOCL1 and CLOCK 2)

that are respectively synchronized with oppositely polarized transitions in level of the data signal (Fig.5 elements 300 and TUNE and column 4 lines 5-18);

second circuitry (Fig.5 elements 300 and 510) configured to sample the data signal (Fig.5 element 510 input, RECEIVE DATA) in a predetermined phase relationship to the first phase-shifted version of the reference clock signal (Fig.5 element 510 input, RECOVERED CLOCK, where the RECEIVERED CLOCK is CLOCK1/CLOCK2) in order to produce a first partial stream of data extracted from the data signal (Fig.5 element 510 output, RECOVERED DATA); and

third circuitry configured to sample the data signal (Fig.5 element 510 input, RECEIVE DATA) in a predetermined phase relationship to the second phase-shifted version of the reference clock signal (Fig.5 element 510 input, RECOVERED CLOCK, where the RECEIVERED CLOCK is CLOCK2/CLOCK1) in order to produce a second partial stream of data extracted from the data signal (Fig.5 element 510 output, RECOVERED DATA).

Kyles et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching the data signal having a data rate that is twice the reference clock signal frequency.

However, Kyles' reference, column 2 lines 17-38 teaches that a divided by N divider (Fig.2 element 116) is placed between the Recovered Clock 114 and Phase Frequency Detect 122 so that the data signal having a data rate that is twice (N times) the reference clock signal frequency (column 2 lines 15-28).

It is desirable to include the divider between the Recovered Clock and Phase Frequency Detect to provide an advantage that permits operation of the PLL control means at a frequency significantly lower than the transmit or receive frequency generated by the VCO. That is, the required frequency of PLL control means operation is reduced by a factor corresponding to the selected divisor. Suitable control voltage scaling is then utilized to operate the VCO at the proper frequency. The use of divider in this fashion permits PLL control circuit operation at a relatively low frequency, compared to the PLL operation without divider. Accordingly, a relatively inexpensive low-frequency PLL control circuit may be utilized.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the divider (Fig.2 element 116) as taught by Kyles et al. into Kyles' Fig.5 circuit by placing the divider between the RECOVERED CLOCK and PHASE DETECT 520 so as to reduce the total system cost.

- With regard claim 16, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 24, Kyles et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching operation phase locked loop circuitry to produce the reference clock signal

However, Fig.2 of Kyles et al. further discloses operation phase locked loop circuitry to produce the reference clock signal (Fig.2 elements 120, 122, 126, 130, 134, 112 and 116). The explanation has been addressed in the above paragraph.

- With regard claim 25, which is an apparatus claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kyles et al. (US 6,008,680) in view of Li et al. (US 6,693,985).

- With regard claim 11, Kyles et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching a Programmable logic device circuitry to implement the clock and data recovery circuit.

However, Li et al. teaches that a Programmable logic device circuitry to implement a clock and data recovery circuit (column 7 line 58 – column 8 line 21).

It is desirable to include a Programmable logic device circuitry to implement a clock and data recovery circuit. The reason for this is if the variety of discrete circuitries of clock and data recovery circuit is implemented into a PLD, the circuit complexity and circuit board size can be reduced so that the system cost can be reduced. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus as taught by Li et al. in which, having a Programmable logic device circuitry to

implement the clock and data recovery circuit, into Kyles' data/clock recovery circuitry so as to reduce the total system cost.

4. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyles et al. (US 6,008,680) and Li et al. (US 6,693,985) as applied to claim 11 above, and further in view of Wang et al. (US 6,292,116).

- With regard claim 12, Kyles et al. and Li et al. disclose all of the subject matter as described in the claim 11 except for specifically teaching

  a) processing circuitry; and

  b) a memory coupled to said processing circuitry.

  However, Wang et al. further teaches a processing circuitry (Fig.1 element 101) and a memory coupled to said processing circuitry (Fig.1 element 105).

  It is desirable to include a processing circuitry and a memory coupled to said processing circuitry in a board. The reason for this is if the memory coupled to said processing circuitry, the programmable and operational execution software can be stored so that the external control circuitry can be eliminated and it reduce the system cost. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus/method as taught by Wang et al. in which, having a processing circuitry and a memory coupled to said processing circuitry, into Kyles et al. and Lis' data/clock recovery circuitry so as to reduce the total system cost.

- With regard claims 13-15, Lee et al. and Li et al. disclose all of the subject matter as described in the claim 11 except for specifically teaching the PLD, the processing circuitry, and the memory will be mounted on a printed circuit board.

  However, Wang et al. further teaches the PLD, the processing circuitry, and the memory will be mounted on a printed circuit board (column 3 lines 19-40).

  It is desirable to mount the PLD, the processing circuitry, and the memory on a printed circuit board for operation in order to reduce the extra wiring and external interface connection so that the system reliability can be improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to mount the PLD, the processing circuitry, and the memory on a printed circuit board as taught by Wang et al. into Lee et al. and Lis' data/clock recovery circuitry so as to reduce the extra wiring and external interface connection so that the system reliability can be improved.

  All other limitation is contained in claims 11 and 12. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

5. Claims 2-10, 17-23 and 26-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang